CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method of at least one of testing, diagnosing, and monitoring an operation of an electronic circuit, said method comprising:

interrupting a clock signal used to provide a clocking for a normal operation of said circuit; and

using a second clock signal to repeatedly cycle through a predetermined cycle of operations for said circuit.

2. The method of claim 1, further comprising:

causing a data signal sequence in said circuit to flow in a reverse direction during the repeated cycling of said predetermined cycle of operation.

3. The method of claim 2, wherein said data signal sequence is reversed by controlling a multiplexer.

4. The method of claim 3, wherein:

said circuit comprises a scan chain of latches;

said reversed data signal sequence occurs in said scan chain of latches; and

said multiplexer interconnects a master flipflop and a slave flipflop in latches that comprise said scan chain.

5. The method of claim 1, further comprising:

collecting data on an emission of photons that occur from said circuit during the repeated cycling of said predetermined cycle of operations.

6. The method of claim 1, further comprising:

prior to said interrupting said clock signal, performing a Built-In Self Test (BIST) sequence on said circuit.

7. The method of claim 6, further comprising:

analyzing a result of said BIST sequence of said circuit.

8. The method of claim 7, further comprising:

beginning an execution of said BIST sequence a second time, wherein said interruption of said interrupting a clock signal occurs at a step in said BIST sequence determined during said analyzing to have a failure.

9. An electronic circuit testing apparatus, comprising:

a first clock signal line to operate an electronic circuit during a normal sequencing of operations;

an interrupt signal line causing said first clock signal to stall in a middle of a cycle; and

a second clock signal line to operate said electronic circuit during a period when said first clock signal is stalled.

10. The apparatus of claim 9, further comprising:

a signal line to cause a data signal sequence in said circuit to flow in a reverse direction during a period said first clock signal is stalled.

11. The apparatus of claim 9, further comprising:

a controller to control said interrupt signal line.

12. The apparatus of claim 9, further comprising:

a controller to control an execution of a Built-In Self Test (BIST) sequence of said electronic circuit.

13. The apparatus of claim 9, further comprising:

a detection module to detect an activity in said electronic circuit.

14. The apparatus of claim 13, wherein said detection module comprises:

a light detector coupled to photomultiplier.

15. The apparatus of claim 14, wherein said light detector detects energy in an infrared light wavelength.

16. The apparatus of claim 15, further comprising:

an image analyzer to analyze images obtained from said light detector.

17. The apparatus of claim 12, further comprising:

a computer module to analyze a result of said BIST sequence.

18. The apparatus of claim 17, wherein the analysis of said BIST sequence comprises a determination of at least one of a failing pattern of said BIST sequence and a failing path.

19. The apparatus of claim 18, wherein said controller causes said BIST sequence to execute to a position in said BIST sequence where said failing pattern has been determined.

20. A signal-bearing medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus to perform a method of at least one of testing, diagnosing, and monitoring an operation of an electronic circuit, said method comprising:

interrupting a clock signal used to provide a clocking for a normal operation of said circuit; and

using a second clock signal to repeatedly cycle through a predetermined cycle of operations for said circuit.

21. The signal-bearing medium of claim 20, said method further comprising at least one of:

causing a data signal sequence in said circuit to flow in a reverse direction during the repeated cycling of said predetermined cycle of operation;

collecting data on an emission of photons that occur from said circuit during the repeated cycling of said predetermined cycle of operations;

prior to said interrupting said clock signal, performing a Built-In Self Test (BIST) sequence on said circuit;

analyzing a result of said BIST sequence of said circuit; and

beginning an execution of said BIST sequence a second time, wherein said interruption of said interrupting a clock signal occurs at a position in said BIST sequence determined during said analyzing to have a failure.

22. An electronic circuit, comprising:

at least one scan chain of latches; and

a mechanism to allow a data flow in said scan chain to be reversed in direction.

23. The electronic circuit of claim 22, wherein each said latch comprises a master flipflop and a slave flipflopand said mechanism to reverse data flow comprises a multiplexer interconnected between said master flipflop and said slave flipflop.

24. An electronic apparatus, comprising:

at least one electronic circuit that includes at least one scan chain of latches and a mechanism corresponding to said at least one scan chain to allow a data flow in said scan chain to be reversed in direction.

25. The electronic apparatus of claim 24, wherein each said latch comprises a master flipflop and a slave flipflop and said mechanism to reverse data flow comprises a multiplexer interconnected between said master flipflop and said slave flipflop.

26. A method of at least one of testing, diagnosing, and monitoring an operation of an electronic circuit, said method comprising:

mounting said electronic circuit such that a photodetector can detect photon emissions due to an operation of said electronic circuit;

exercising said electronic circuit with a built-in-self-test sequence;

determining a position in said built-in-self-test sequence where a failure occurs; and

recycling a plurality of times through a sequence of said built-in-self-test sequence at said determined position in said built-in-self-test, said photodetector detecting a photon emission due to activity of said electronic circuit during said recycling, said recycling thereby causing an amplification effect of said photon emission during said recycling.

27. The method of claim 26, wherein said recycling is caused by:

interrupting a clock signal used to provide a clocking for a normal operation of said circuit; and

using a second clock signal to repeatedly cycle through a predetermined cycle of operations for said circuit.

28. The method of claim 26, wherein said electronic circuit comprises at least one scan chain of latches, said method further comprising:

causing a reverse in direction of a signal flow through said scan chain of latches during said recycling.

29. The method of claim 28, wherein said latches comprise a master flipflop and a slave flipflop and said causing a reverse in direction is due to activation of a multiplexer that interconnects said master flipflop and said slave flipflop.

30. The method of claim 26, further comprising:

analyzing said photon emission to determine a failed component in said electronic circuit.